Application Note

DESIGN CONSIDERATIONS WHEN USING THE CS7410 INTERNAL DAC

1. INTRODUCTION

The internal Delta-Sigma modulator inside the CS7410 allows the conversion of the digital PCM data inside the CS7410 to analog audio. The Delta-Sigma modulator inside the CS7410 converts the PCM data to over-sampled one-bit data. This data is output differentially on the LP/LN and RP/RN pins, low pass filtered and amplified to drive an external set of headphones. In the context of the familiar CMOS DAC, this approach separates the digital and analog portions of the DAC. The digital portion resides inside the CS7410 and the analog portion is implemented using discrete components.

2. DESIGN CONSIDERATIONS

In order to achieve the best possible performance from the internal Delta-Sigma modulator, the recommended circuit diagram shown in figure 4 or 6 and the recommended layout shown in figure 5 should be used. Failure to follow the recommended circuit design and layout can result in both poor overall dynamic range and distortion. There are several areas to pay careful attention to when designing your system.

2.1 Power Supply Routing and Filtering

For cost reasons, the analog output circuit operates from the digital 1.8 V and 3.3 V power supplies. Since these supplies are also used to power all the digital circuitry, they must be carefully routed and filtered to prevent digital noise from corrupting the analog audio.

For best audio performance, the entire analog circuitry, including the 74AC74 logic part, should be connected to the same filtered 3.3 V supply and filtered ground. This filtered 3.3 V supply is identified as IDAC_3.3V in the attached schematic. The corresponding filtered analog ground node is identified as IDAC_GND in the attached schematic. The connecting traces for IDAC_3.3V and IDAC_GND should be routed straight from the 3.3 V regulator pins and not tapped anywhere near the CS7410 or any other logic circuit. The IDAC_3.3V/IDAC_GND filter components should be placed as close to the analog circuit as possible, not close to the 3.3 V regulator. Be careful to use high quality ferrite beads on leads as indicated in the attached circuit diagram. Failure to use the proper filtering will degrade the audio performance.

2.2 Reference Voltage Generation for the Op-Amp

The reference voltages for the headphone driver op-amps are generated from the 1.8 V digital supply and must be carefully designed and laid out. The filtered 1.8 V supply is identified as REF_VDD1 and REF_VDD2 in the attached schematic. It is very important to use separate filter circuits for each op-amp. Otherwise, the signal-to-idle-channel noise (or cross-talk) specification may degrade. Corresponding to REF_VDD1 and

REF_VDD2 are 2 other filtered ground nodes, called REF_GND1 and REF_GND2 that should be carefully treated. The connecting traces for REF_VDD1 / REF_GND1 and REF_VDD2 / REF_GND2 should be routed straight from the 1.8 V regulator pins and not tapped anywhere near the CS7410 or any other logic circuit. The filter components should be placed as close to the analog circuit as possible, not close to the 1.8 V regulator. Be careful to use high quality ferrite beads on leads as indicated in the attached circuit diagram. Failure to use the proper filtering will degrade the audio performance.

Each active device in the analog circuit requires good local power supply decoupling for correct operation. The 74AC74 requires a parallel 0.1/0.01 µF capacitor pair placed as close to chip as possible and connected to the VCC and GND pins without vias. The op-amp requires a 0.1 µF capacitor placed as close as possible to the chip and connected to the VDD/VSS pins without vias. The CS7410 also requires careful decoupling on it's I/O supply pins. Each I/O supply pair should be decoupled with a 0.1 µF capacitor placed as close to the chip as possible and connected to the chip pins with no vias.

2.3 Signal Routing

The high frequency one-bit data from the CS7410 DAC_LP, DAC_RP, and the PCM_XCLK signal must be routed carefully between the CS7410 and the 74AC74 to in order to preserve signal integrity. Excessive ringing, capacitive loading or jitter on these signals can degrade the overall audio performance. In general, these signals should be kept as short as possible and routed over ground plane. Please refer to the attached layout diagram for preferred layout practices.

All the analog signals around the op-amp should be routed away from any digital signal traces. Analog routes should be short and routed on the top layer in a 2-layer design. The bottom layer should be flooded with continuous ground plane to create a low impedance ground return path and signal reference.

3. PERFORMANCE

Table 1 shows the performance of the reference design presented in this document as achieved with a modified SA03 development board. Plots corresponding to these measurements are shown in figures 1, 2, and 3 respectively. All measurements are taken using an Analog Precision System 2 with an AES-17 filter.

Parameter	Typical	Unit
THD+N (Note 1)	-75	dB
Dynamic Range (Note 2)	79	dB
Crosstalk (Note 3)	72	dB

Table 1: Performance of Reference Circuit 1

1) THD+N measured from 20-20kHz with an input of 1kHz, 0dBFS and the volume set to 1dB below output clipping.

2) Input signal of 1kHz, -60dBFS and volume setting same as in note 1.

3) Input on the left channel of 1kHz, 0dB and DC silence on the right and volume setting same as in note 1.

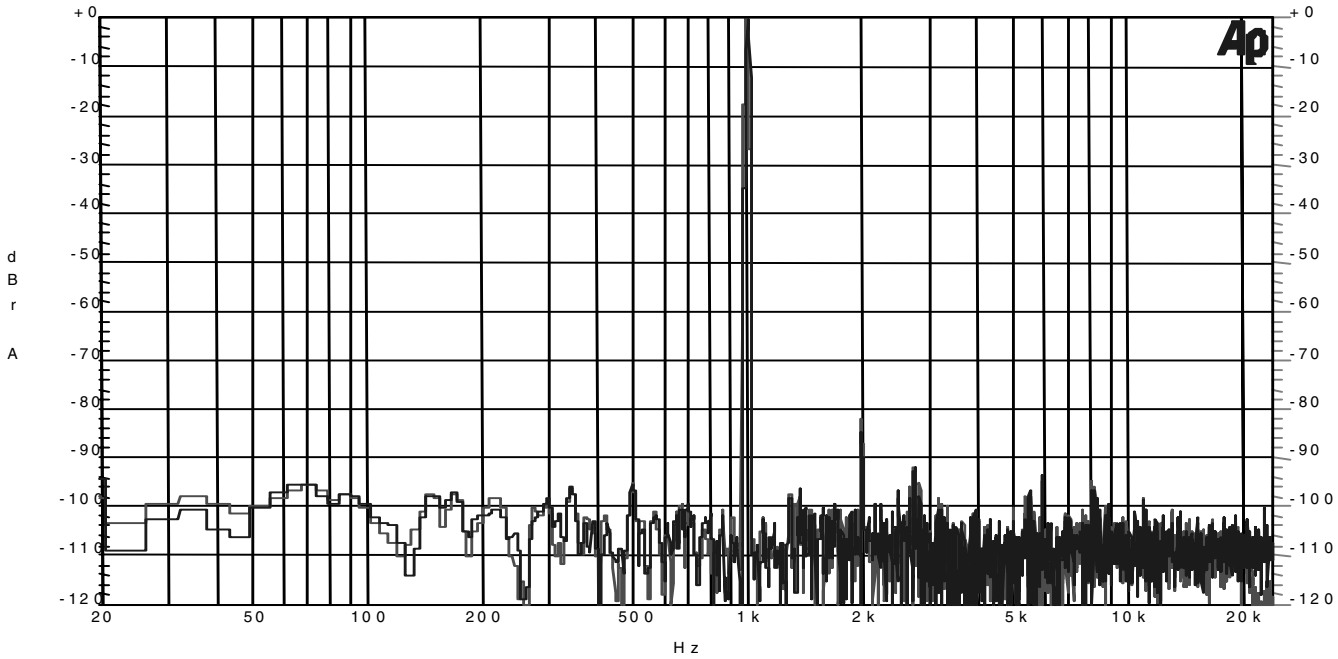

Figure 1. THD+N

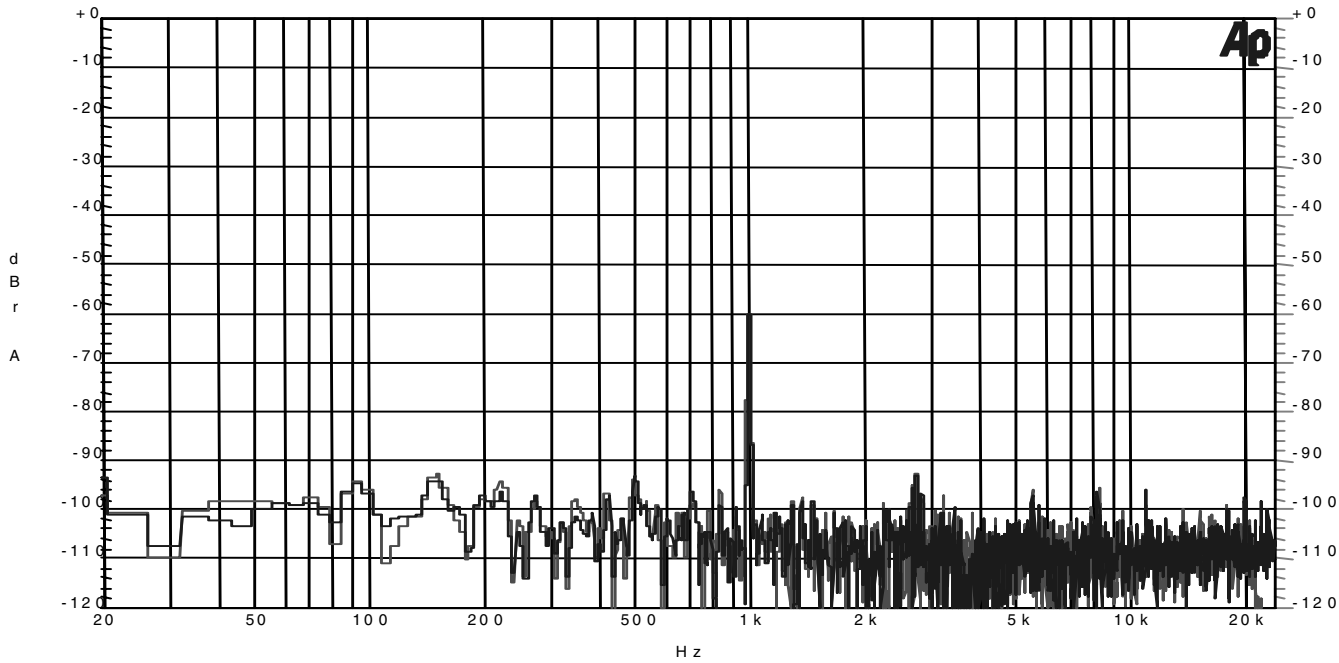

Figure 2. Dynamic Range

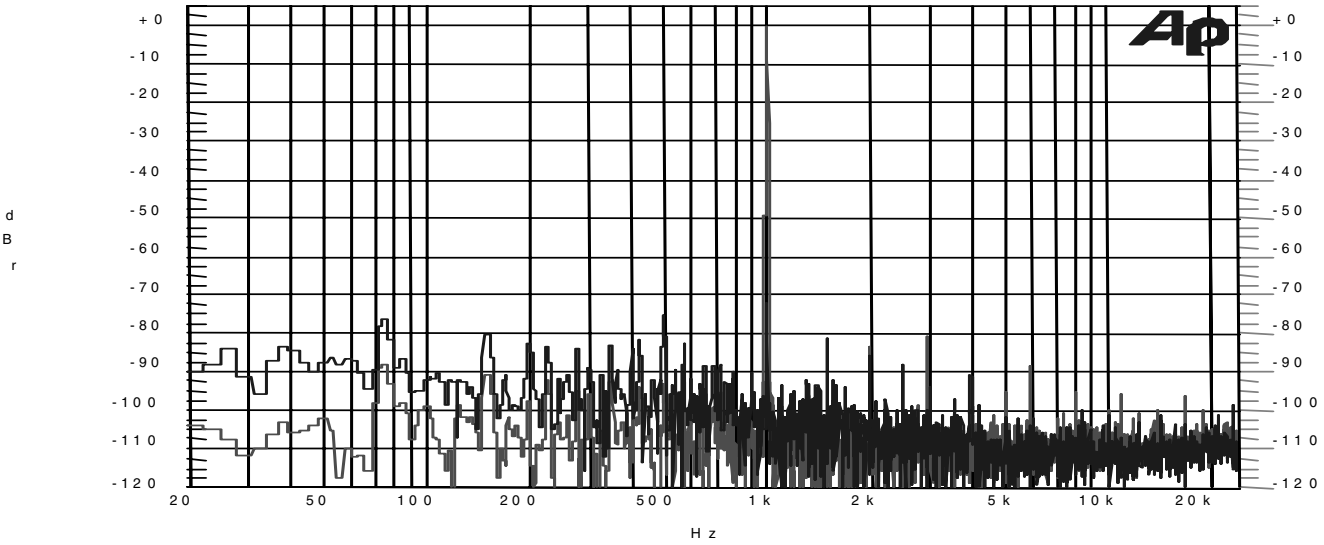

Figure 3. Crosstalk

4. IMPLEMENTATION

Included in this application note is a recommended schematic and board layout for the entire internal DAC audio section for the CS7410. PADS / PowerLogic format schematics and PCB layout files are available from Cirrus Logic.

A second schematic detailing the use of a two-pole filter is also included. This filter design may increase the performance of the CS7410's converter beyond the numbers published here.

Important!

Please be aware that the performance of the circuit described here is dependent on the components used and board layout. The guidelines listed in previous sections of this document are absolutely critical to follow if one is to show similar results. Cirrus Logic provides **free** design review services for customers designing with any of our products, including schematic and board layout review. Please contact your local FAE or sales office to set up a formal review. For your convenience, our web site contains a Cirrus Logic sales office locator at http://www.cirrus.com.

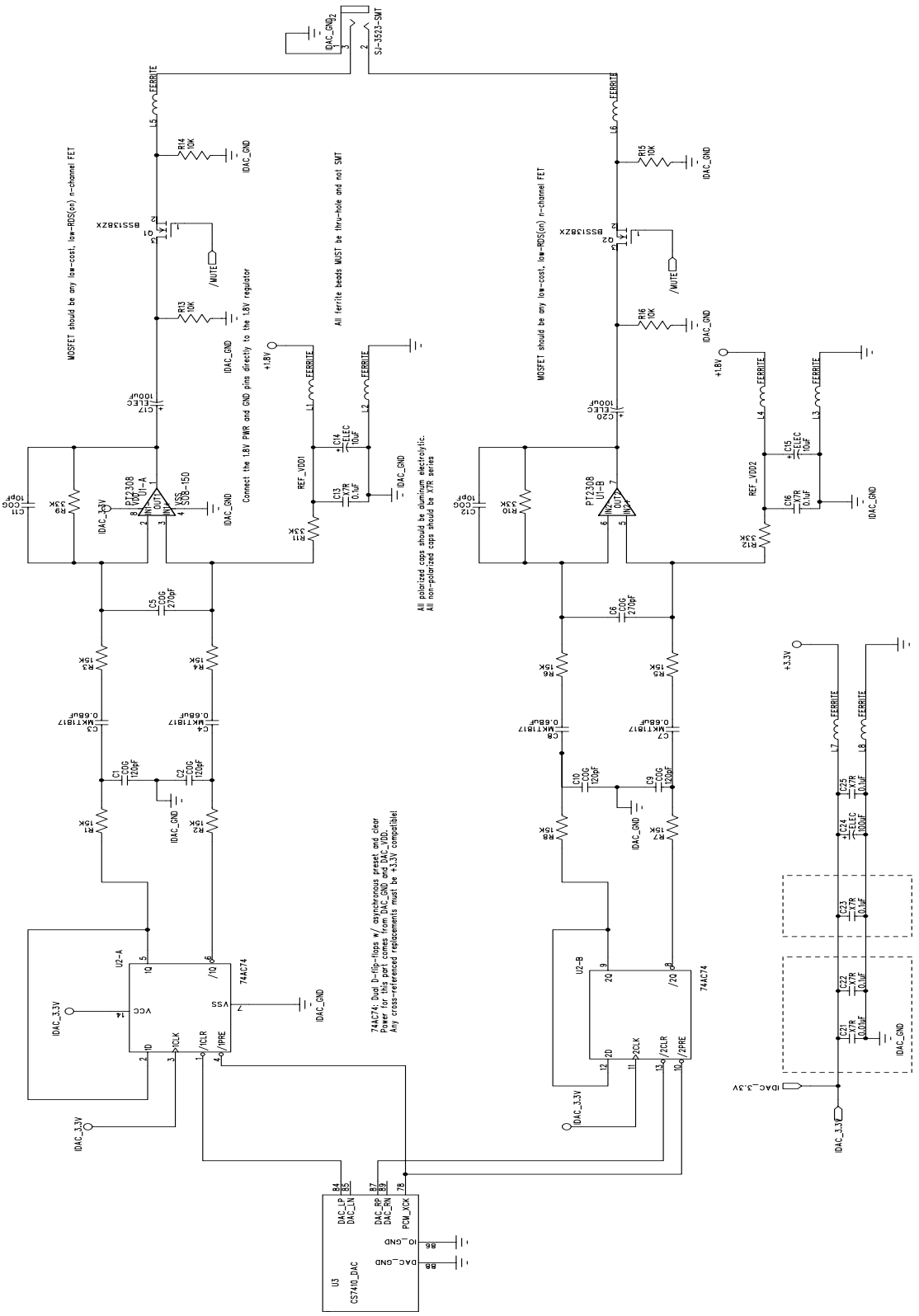

Figure 4. Schematic 1

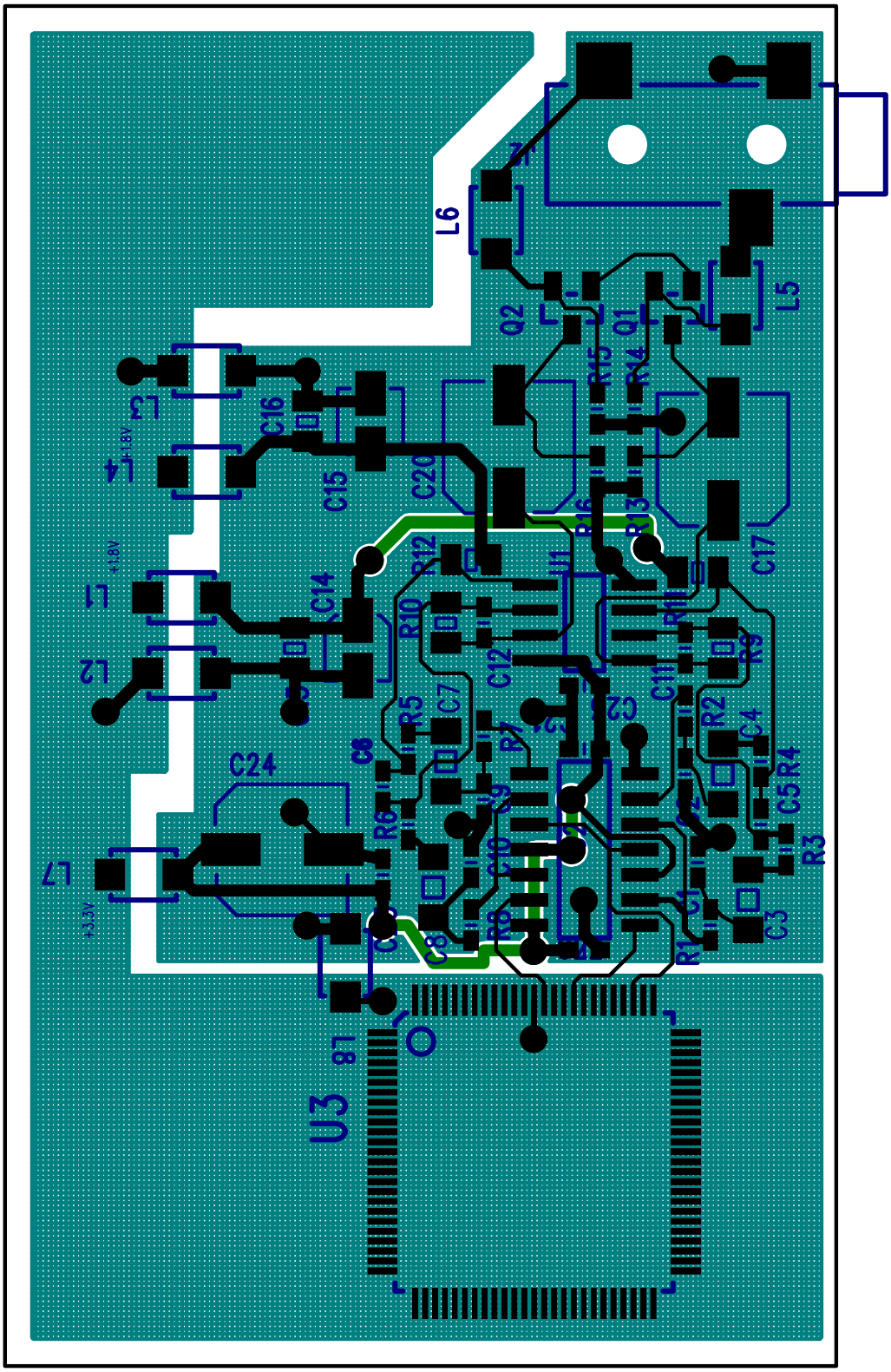

Figure 5. PCB Stencil

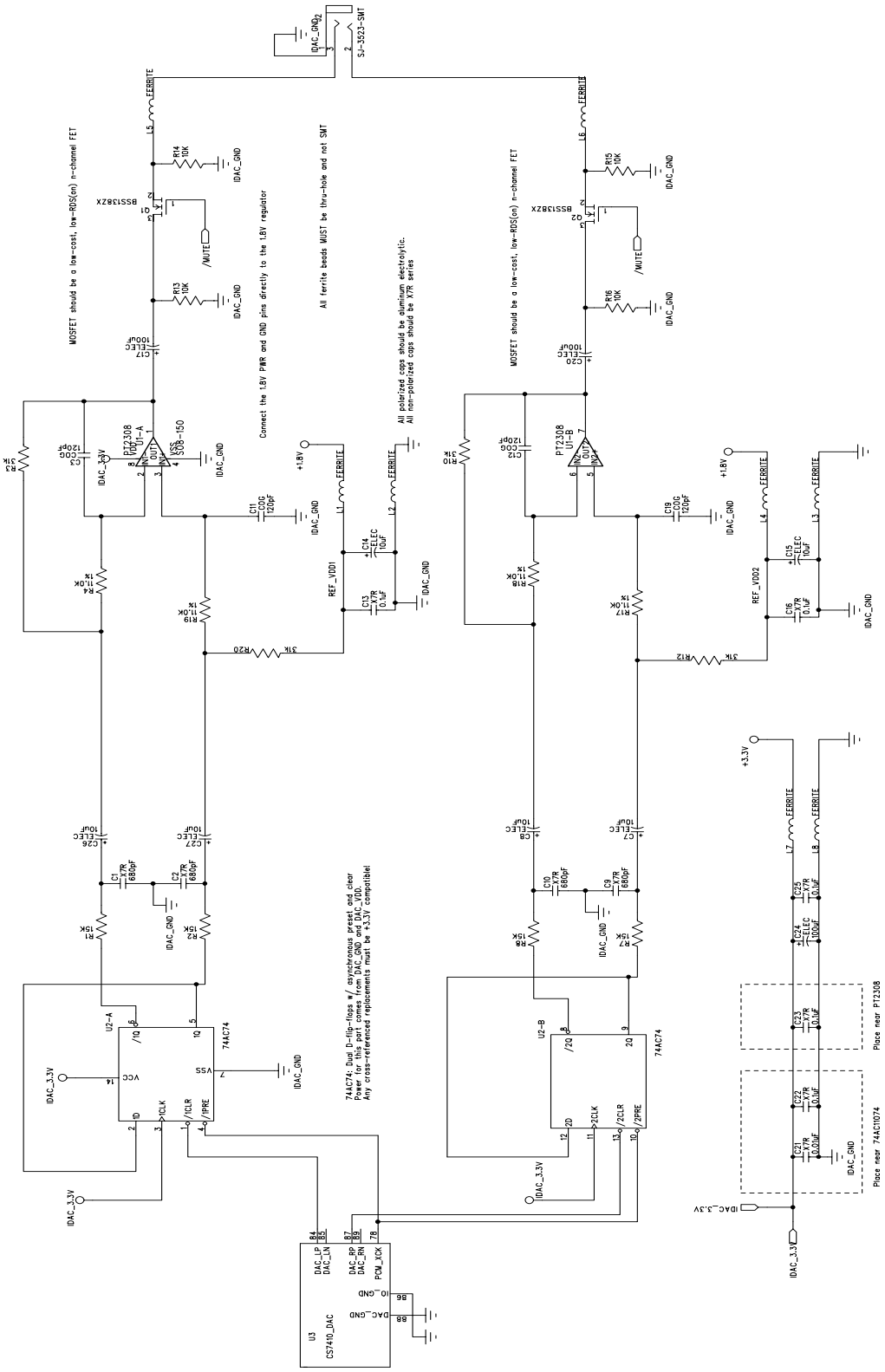

Figure 6. Alternative Schematic: 2-Pole Butterworth Filter at 30kHz with G=2.0

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• Notes •


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